Attorney Docket No. 5646-113 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Declan McDonagh et al.
Serial No.: To Be Assigned
Filed: Concurrently Herewith
For: CLOCK SIGNAL GENERATORS HAVING PROGRAMMABLE FULL-PERIOD CLOCK SKEW CONTROL AND METHODS OF GENERATING CLOCK SIGNALS HAVING PROGRAMMABLE SKEWS

Date: August 26, 2003

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Sir:

Attached is a list of documents on Form PTO-1449, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the waiver by the U.S. Patent and Trademark Office of requirements under 37 C.F.R. § 1.98(a)(2)(i) for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003.

It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

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CERTIFICATE OF MAILING UNDER 37 CFR § 1.10

"Express Mail" mailing label number EV318420695US
Date of Deposit: August 26, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Mail Stop Patent Application, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Candi L. Riggs

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)	Attorney Docket Number 5646-113	Serial No. To Be Assigned
	Applicants: Declan McDonagh et al.	
	Filing Date: Concurrently Herewith	Group

U. S. PATENTS & PATENT APPLICATION PUBLICATIONS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1	6,597,212	7/22/03	Wang et al.	327	117	
	2	6,525,584	2/25/03	Seo et al.	327	276	
	3	6,509,773	1/21/03	Buchwald et al.	327	247	
	4	6,466,098	10/15/02	Pickering	331	25	
	5	6,433,645	8/13/02	Mann et al.	331	18	
	6	6,388,478	5/14/02	Mann	327	113	
	7	6,384,653	5/7/02	Broome	327	247	
	8	6,359,486	3/19/02	Chen	327	231	
	9	6,329,859	12/11/01	Wu	327	291	
	10	6,271,702	8/7/01	Stansell	327	295	
	11	6,111,445	8/29/00	Zerbe et al.	327	231	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes | No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	12	Rabaey, Jan M., "Synchronization at the System Level," Digital Integrated Circuits, A Design Perspective, Prentice-Hall, Inc., pp. 540-543
	13	"High-Speed Multi-Phase PLL Clock Buffer," Cypress Semiconductor Corporation, Revised July 25, 2003, 14 pages

EXAMINER _____ DATE CONSIDERED

*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.